A Bibliography of Publications on Visual Instruction Sets

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Title word cross-reference

2 [IM99, Lee96, OWJF98]. **2.0** [LHxx].

3 [Hal97]. **3-D** [Hal97]. **3DNow** [OWJF98, OFW99, Adv00a, BN99, IM99, Fom00].

64-bit [LHxx].

7100LC [Ano95, BBJ+95, BKQW95, LBLS95, Smi94]. **712/60** [Smi94]. **7300LC** [BT97].

accelerate [TONH96]. **Accelerates** [DDHS00]. **Accelerating** [DDC+98, Lee96, Sun96a]. **achieve** [Smi94]. **Across** [DDC+98]. **algorithms** [TONH96]. **Alpha** [RRM96]. **Alternatives** [Ano98]. **AltiVec** [DDC+98, DDHS00, Fit01, Ful98, Mot98, Mot99b, Mot99a, Mot99c, Phi98]. **Alto** [IEE98]. **AMD** [Adv00b, Hal97, IM99, OWJF98, OFW99, Pou98]. **AMD-K62-E** [Adv00b]. **Analysis** [IM99, SB01]. **Apple** [Fit01]. **Application** [Hun00, PW96]. **Architecture** [Hsu01, LHxx, MPW97, OFW99, PW96, Phi98, TO96]. **architectures** [Ano96a]. **Aspects** [Hsu01]. **Assembly** [Sun00]. **Auditorium** [IEE98]. **August** [IEE96, IEE97, IEE98]. **Automatically** [BGGT01].

based [BM00, Hun00]. **Better** [Ano97a]. **Beyond** [Hal97]. **bit** [LHxx]. **Black** [Ben95]. **Blazing** [Tho98]. **Blinn** [Bli97]. **breakthroughs** [Smi94]. **Briefs** [GL97]. **Bugs** [Ben95]. **builds** [Pou98]. **Built** [Pea95]. **Built-In** [Pea95]. **Business** [BEM95, GL97]. **BYTE** [Ano96a, Ano96b].

References

Aberdeen:2001:EFM

[AB01] Douglas Aberdeen and Jonathan Baxter. Emmerald: a fast matrix-matrix multiply using Intel's SSE instructions. *Concurrency and Computation: Practice and Experience*, 13(2):103–119, February 2001. CODEN CCPEBO. ISSN 1532-0626 (print), 1532-0634 (electronic). URL `http://www3.interscience.wiley.com/cgi-bin/abstract/77004416/START; http://www3.interscience.wiley.com/cgi-bin/fulltext?ID=77004416&PLACEBO=IE.pdf`.

AMD:2000:TM

[Adv00a] Advanced Micro Devices, Inc., One AMD Place, P.O. Box 3453, Sunnyvale, California, USA. *3DNow! Technology Manual*, March 2000. x + 62 pp. URL `http://www.amd.com/products/epd/processors/6.32bitproc/8.amdk6fami/26.amdk62e/21928/21928.pdf`. Order number 21928G/0.

AMD:2000:AKE

[Adv00b] Advanced Micro Devices, Inc., One AMD Place, P.O. Box 3453, Sunnyvale, California, USA. *AMD-K62-E+ Embedded Processor Data Sheet*, September 2000. xxii + 346 pp. URL `http://www.amd.com/products/epd/processors/6.32bitproc/8.amdk6fami/28.amdk62e/23542/23542a.pdf`. Order number 23542A/0.

Abel:1997:IHQ

[AJ97] James C. Abel and Michael A. Julier. Implementation of a high quality Dolby digital decoder using MMX technology. *Intel Technology Journal*, (Q3):11, 1997. URL `http://developer.intel.com/technology/itj/q31997/articles/art_3.htm; http://developer.intel.com/technology/itj/q31997/pdf/decoder.pdf`.

Anonymous:1994:NPd

[Ano94] Anonymous. New Products. *Datamation*, 40(4):85–??, February 15, 1994. CODEN DTMNAT. ISSN 0011-6963.

Anonymous:1995:OIP

[Ano95] Anonymous. Overview of the implementation of the PA 7100LC multimedia enhancements. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):66, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_66.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Anonymous:1996:BRW

[Ano96a] Anonymous. BYTE readers write about new server architectures, Windows NT issues, MMX programming, and "free PCs". *Byte Magazine*, 21(10):19–??, October 1996. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Anonymous:1996:IBRa

[Ano96b] Anonymous. INBOX — BYTE readers sound off on electric money, Internet commerce and privacy, programming for Intel's MMX, and praise the core of BYTE. *Byte Magazine*, 21(9):19–??, September 1996. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Anonymous:1997:BFS

[Ano97a] Anonymous. Better in fits and starts — we test a new Pentium hopped up with Intel's MMX. *Byte Magazine*, 22(2):26–??, February 1997. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Anonymous:1997:JHF

[Ano97b] Anonymous. Just how fast are those new MMX chips? *Byte Magazine*, 22(2):26–??, February 1997. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Anonymous:1997:MPD

[Ano97c] Anonymous. MMX power for desktop PCs: We look at 10 Pentium systems souped-up with MMX technology. *Byte Magazine*, 22(7):106–??, July 1997. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Anonymous:1997:SIM

[Ano97d] Anonymous. Special issue on MMX technology. *Intel Technology Journal*, (Q3), 1997. URL `http://developer.intel.com/technology/itj/q31997.htm`.

Anonymous:1998:MA

[Ano98] Anonymous. MMX alternatives. *Byte Magazine*, 23(7):26–??, July 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Atkins:1996:PSP

[AS96] Mark Atkins and Ramesh Subramaniam. PC software performance tuning. *Computer*, 29(8):47–54, August 1996. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic).

Bass:1995:DMP

[BBJ+95] Mick Bass, Terry W. Blanchard, D. Douglas Josephson, Duncan Weir, and Daniel L. Halperin. Design methodologies for the PA 7100LC microprocessor. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46 (2):23–35, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_23.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Bowers:1995:DLC

[BEM95] Dennis A. Bowers, Gerard M. Enkerlin, and Karen L. Murillo. Development of a low-cost, high-performance, multiuser business server system. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):79–84, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_79.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Benzel:1995:BBW

[Ben95] Jack D. Benzel. Bugs in black and white: Imaging IC logic levels with voltage contrast. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):102–106, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_1b.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Bik:2001:AEI

[BGGT01] Aart J. C. Bik, Milind Girkar, Paul M. Grey, and Xinmin Tian. Automatically exploiting implicit parallelism. *Dr. Dobb's Journal of Software Tools*, 26(7):28, 30, 32–34, July 2001. CODEN DDJOEB. ISSN 1044-789X. URL `http://www.ddj.com/ftp/2001/2001_07/parallel.txt`.

Bass:1995:PMC

[BKQW95] Mick Bass, Patrick Knebel, David W. Quint, and William L. Walker. The PA 7100LC microprocessor: A case study of IC design decisions in a competitive environment. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):12–22, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_12.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Blinn:1997:JBC

[Bli97] James F. Blinn. Jim Blinn's corner: Fugue for MMX. *IEEE Computer Graphics and Applications*, 17(2): 88–93, March/April 1997. CODEN ICGADZ. ISSN 0272-1716 (print), 1558-1756 (electronic). Makes several cogent comments about deficiencies in the Intel MMX pixel-processing instruction set [PWW97] for use in image compositing.

Brooks:2000:VBC

[BM00] David Brooks and Margaret Martonosi. Value-based clock gating and operation packing: dynamic strate-

gies for improving processor power and performance. *ACM Transactions on Computer Systems*, 18(2): 89–126, May 2000. CODEN ACSYEC. ISSN 0734-2071 (print), 1557-7333 (electronic). URL `http://www.acm.org/pubs/citations/journals/tocs/2000-18-2/p89-brooks/`.

Bush:1999:CEE

[BN99] Jonathan Bush and Timothy S. Newman. The cutting edge: Effectively utilizing 3DNow! in Linux. *Linux Journal*, 68:??, December 1999. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic). URL `http://noframes.linuxjournal.com/lj-issues/issue68/3685.html`.

Blanchard:1997:PMH

[BT97] T. W. Blanchard and P. G. Tobin. The PA 7300LC microprocessor: a highly integrated system on a chip. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 48(3):43–47, June 1997. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/97jun/ju97a6.htm`.

Diefendorff:1998:ATA

[DDC+98] K. Diefendorff, P. Dubey, R. Chochsprung, et al. AltiVec technology: Accelerating media processing across the spectrum. In IEEE [IEE98], page ?? ISBN ???? LCCN ????

Diefendorff:2000:AEP

[DDHS00] Keith Diefendorff, Pradeep K. Dubey, Ron Hochsprung, and Hunter Scales. AltiVec extension to PowerPC accelerates media processing. *IEEE Micro*, 20(2):85–95, March/April 2000. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi2000/pdf/m2085.pdf`.

Drongowski:2000:TM

[Dro00] Paul J. Drongowski. Translating MMX. *Computer*, 33(3):43, March 2000. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `http://dlib.computer.org/co/books/co2000/pdf/r3040.pdf`.

Fite:2001:FLA

[Fit01] Matthew Fite. First look at an Apple G4 with the AltiVec processor. *Linux Journal*, 86:108, 110–111, 114, 116, 118, June 2001. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic). URL `http://noframes.linuxjournal.com/lj-issues/issue86/4584.html`.

Fomitchev:1999:MTC

[Fom99] Max I. Fomitchev. MMX technology code optimization. *Dr. Dobb's Journal of Software Tools*, 24(9):38, 40, 42–46, 48, September 1999. CODEN DDJOEB. ISSN 1044-789X. URL `http://www.ddj.com/ftp/1999/1999_09/mmx.txt`; `http://www.ddj.com/ftp/1999/1999_09/mmx.zip`.

Fomitchev:2000:ORT

[Fom00] Max I. Fomitchev. Optimizing 3Dnow! real-time graphics. *Dr. Dobb's Journal of Software Tools*,

25(8):40, 42–46, August 2000. CODEN DDJOEB. ISSN 1044-789X. URL `http://www.ddj.com/ftp/2000/2000_08/3dnow.txt; http://www.ddj.com/ftp/2000/2000_08/3dnow.zip`.

Fuller:1998:MAT

[Ful98] Sam Fuller. Motorola's AltiVec technology. Technical Report ALTIVECWP/D, Motorola Corporation, Phoenix, AZ, USA, 1998. 4 pp. URL `http://a1888.g.akamai.net/7/1888/787/83ade987b85512/www.motorola.com/SPS/PowerPC/teksupport/teklibrary/papers/altivec_wp.pdf`.

Grosky:1997:NSV

[GL97] William Grosky and Anne C. Lear. In the news: Smart but vulnerable; transitioning to digital TV; gaining voices; business briefs; technology notes; phoning the Web; converging competition; Intel presents MMX — and another upgrade dilemma; want more information? *IEEE MultiMedia*, 4(1):12–16, January–March 1997. CODEN IEMUE4. ISSN 1070-986X (print), 1941-0166 (electronic). URL `http://dlib.computer.org/mu/books/mu1997/pdf/u1012.pdf`.

Gove:2006:SSU

[GV06] Darryl Gove and Geetha Vallabhanen. Sun Studio: Using VIS instructions to speed up key routines. *Sun Developer Network*, January 5, 2006. URL `http://developers.sun.com/prodtech/cc/articles/vis.html`.

Halfhill:1997:BMN

[Hal97] Tom R. Halfhill. Beyond MMX — new 3-D power of AMD, Centaur, and Cyrix chips will challenge Intel. *Byte Magazine*, 22(12):87–??, December 1997. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Hsu:2001:CAS

[Hsu01] John Y. Hsu. *Computer Architecture: Software Aspects, Coding, Hardware*. CRC Press, 2000 N.W. Corporate Blvd., Boca Raton, FL 33431-9868, USA, 2001. ISBN 0-8493-1026-1, 1-351-83604-8, 1-4200-4110-X (e-book). 427 pp. LCCN A76.9.A73 H758 2001. US$89.95, UK£59.99.

Hunter:2000:EPG

[Hun00] Craig A. Hunter. An evaluation of PowerMac G4 systems for FORTRAN-based scientific computing with application to computational fluid dynamics simulation. Technical report, NASA Langley Research Center, Configuration Aerodynamics Branch, Hampton, VA, USA, July 2000. URL `http://ad-www.larc.nasa.gov/~cah/NASA_G4_Study.pdf`.

IEEE:1996:HCV

[IEE96] IEEE, editor. *Hot chips VIII: symposium record: Stanford University, Stanford, California, August 18–20, 1996*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1996. ISBN ???? LCCN ????

IEEE:1997:HCI

[IEE97] IEEE, editor. *Hot Chips IX: Stanford University, Stanford, California, August 24–26, 1997*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1997. ISBN ???? LCCN ????

IEEE:1998:HCC

[IEE98] IEEE, editor. *Hot chips 10: conference record: August 16–18, 1998, Memorial Auditorium, Stanford University, Palo Alto, California*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1998. ISBN ???? LCCN ????

Iordache:1999:ARS

[IM99] Cristina Iordache and David W. Matula. Analysis of reciprocal and square root reciprocal instructions in the AMD K6-2 implementation of 3DNow! *Electronic Notes in Theoretical Computer Science*, 24:34–62, 1999. CODEN ???? ISSN 1571-0661.

Jennings:1998:MCS

[JC98] Matthew D. Jennings and Thomas M. Conte. Mobile computing: Subword extensions for video processing on mobile systems. *IEEE Concurrency*, 6(3):13–16, July/September 1998. CODEN IECMFX. ISSN 1092-3063 (print), 1558-0849 (electronic). URL `http://dlib.computer.org/pd/books/pd1998/pdf/p3013.pdf`.

Kagan:1996:PMF

[Kag96] Michael Kagan. The P55C microarchitecture — the first implementation of MMX technology. In IEEE [IEE96], pages 157–162. ISBN ???? LCCN ????

Khazam:1996:PSI

[KB96] Jonathan Khazam and Bev Bachmayer. Programming strategies for Intel's MMX. *Byte Magazine*, 21(8): 63–64, August 1996. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Kagan:1997:MMP

[KGOL97] Michael Kagan, Simcha Gochman, Doron Orenstien, and Derrick Lin. MMX microarchitecture of Pentium processors with MMX technology and Pentium II microprocessors. *Intel Technology Journal*, (Q3):8, 1997. URL `http://developer.intel.com/technology/itj/q31997/articles/art_4.htm`; `http://developer.intel.com/technology/itj/q31997/pdf/micro.pdf`.

Lee:1995:RTS

[LBLS95] Ruby B. Lee, John P. Beck, Joel Lamb, and Kenneth E. Severson. Real-time software MPEG video decoder on multimedia-enhanced PA 7100LC processors. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):60–68, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_60.pdf`; `http://www.hp.com/hpj/toc-04-95.html`.

Lee:1996:SPM

[Lee96] Ruby B. Lee. Subword parallelism with MAX-2: Accelerating media

processing with a minimal set of instruction extensions supporting efficient subword parallelism. *IEEE Micro*, 16(4):51–59, July/August 1996. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Lee:19xx:BME

[LHxx] Ruby Lee and Jerry Huck. 64-bit and multimedia extensions in the PA-RISC 2.0 architecture. Technical report, Hewlett–Packard Company, 19410 Homestead Road, Cupertino, CA 95014, USA, 19xx. URL `http://www.hp.com/computing/framed/technology/micropro/architecture/docs/pa2go3.html`.

Maher:1996:MIS

[Mah96] Robert Maher. Multimedia instruction set extensions for a sixth-generation x86 processor. In IEEE [IEE96], pages 163–170. ISBN ???? LCCN ????

Modi:1997:PIC

[Mod97] Nimish Modi. The PentiumAE II CPU: A high performance dynamic execution processor with MMX technology. In IEEE [IEE97], page ?? ISBN ???? LCCN ????

Motorola:1998:ATP

[Mot98] Motorola Corporation, Phoenix, AZ, USA. *AltiVec Technology Programming Environments Manual*, November 1998. 350 pp. Order number ALTIVECPEM/D 11/1998 Rev. 0.1.

Motorola:1999:ATP

[Mot99a] Motorola Corporation, Phoenix, AZ, USA. *AltiVec Technology Programming Interface Manual*, June 1999. 262 pp. Order number ALTIVECPIM/D 6/1999 Rev. 0.

Motorola:1999:APE

[Mot99b] Motorola, Inc. AltiVec programming examples. World-Wide Web document., December 9, 1999. URL `http://www.motorola.com/SPS/PowerPC/AltiVec/CodeMain.html`.

Motorola:1999:ATT

[Mot99c] Motorola, Inc. AltiVec technology tour. World-Wide Web document., December 9, 1999. URL `http://www.motorola.com/SPS/PowerPC/AltiVec/technology.html`.

Mittal:1997:MTA

[MPW97] Millind Mittal, Alex Peleg, and Uri Weiser. MMX technology architecture overview. *Intel Technology Journal*, (Q3):12, 1997. URL `http://developer.intel.com/technology/itj/q31997/articles/art_2.htm; http://developer.intel.com/technology/itj/q31997/pdf/archite.pdf`.

Oberman:1999:ATA

[OFW99] Stuart Oberman, Greg Favor, and Fred Weber. AMD 3DNow! technology: Architecture and implementations. *IEEE Micro*, 19(2): 37–48, March/April 1999. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://dlib.computer.org/mi/books/mi1999/pdf/m2037.pdf; http://www.computer.org/micro/mi1999/m2037abs.htm`.

Oberman:1998:ATK

[OWJF98] Stuart Oberman, Fred Weber, Norbert Juffa, and Greg Favor. AMD 3DNow! technology and the K6-2 microprocessor. In IEEE [IEE98], pages 245–254. ISBN ???? LCCN ????

Pearson:1995:LCH

[Pea95] Roger A. Pearson. A low-cost, high-performance PA-RISC workstation with built-in graphics, multimedia, and networking capabilities. *Hewlett-Packard Journal: technical information from the laboratories of Hewlett-Packard Company*, 46(2):6–11, April 1995. CODEN HPJOAX. ISSN 0018-1153. URL `http://www.hp.com/hpj/95apr/apr95_6t.pdf; http://www.hp.com/hpj/toc-04-95.html`.

Phillip:1998:ATS

[Phi98] Mike Phillip. AltiVec technology: A second generation SIMD microprocessor architecture. In IEEE [IEE98], page ?? ISBN ???? LCCN ????

Pournelle:1998:WJB

[Pou98] Jerry Pournelle. From the workbench — Jerry builds a new system that uses AMD's K6 MMX enhanced chip. *Byte Magazine*, 23 (1):123–??, January 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Peleg:1996:MTE

[PW96] Alex Peleg and Uri Weiser. MMX technology extension to the Intel architecture — improving multimedia and communications application performance by 1.5 to 2 times. *IEEE Micro*, 16(4):42–50, July/August 1996. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Peleg:1997:IMM

[PWW97] Alex Peleg, Sam Wilkie, and Uri Weiser. Intel MMX for multimedia PCs. *Communications of the ACM*, 40(1):24–38, January 1997. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL `http://www.acm.org/pubs/citations/journals/cacm/1997-40-1/p25-peleg/`. See also Blinn's comments [Bli97] about MMX instruction set deficiencies.

Ramirez:1999:OIM

[Ram99] Ariel Ortiz Ramirez. An overview of Intel's MMX technology. *Linux Journal*, 61:??, May 1999. CODEN LIJOFX. ISSN 1075-3583 (print), 1938-3827 (electronic).

Rubinfeld:1996:MVI

[RRM96] Paul Rubinfeld, Bob Rose, and Michael McCallig. Motion video instruction extensions for alpha. Technical report, Semiconductor Engineering Group, 77 Reed Road, HLO2-3/D11 Hudson, MA 01749, USA, October 18, 1996. URL `http://www.digital.com/semiconductor/alpha/papers/pmvi.pdf`.

Strey:2001:PAI

[SB01] Alfred Strey and Martin Bange. Performance analysis of Intel's

MMX and SSE: A case study. *Lecture Notes in Computer Science*, 2150:142–??, 2001. CODEN LNCSD9. ISSN 0302-9743 (print), 1611-3349 (electronic). URL `http://link.springer-ny.com/link/service/series/0558/bibs/2150/21500142.htm; http://link.springer-ny.com/link/service/series/0558/papers/2150/21500142.pdf`.

Scherer:1999:OTW

[SGJ+99] Alisa Scherer, Michael Golden, Norbert Juffa, Stephan Meier, Stuart Oberman, Hamid Partovi, and Fred Weber. An out-of-order three-way superscalar multimedia floating-point unit. In *1999 IEEE International Solid-State Circuits Conference*, page ?? IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 1999. ISBN 0-7803-5129-0. LCCN ????

Smith:1994:PWA

[Smi94] Ben Smith. Power workstation at a Pentium price: The HP 9000 Series 700 Model 712/60 uses innovative hardware packaging and the superscalar PA-7100LC CPU to achieve breakthroughs in low cost and high performance for a Unix workstation. *Byte Magazine*, 19(7):161–??, July 1994. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Sun:1996:ACN

[Sun96a] Sun Microsystems. Accelerating core networking functions using the UltraSPARC VIS instruction set. Technical Report WPR-0013, Sun Microsystems, 901 San Antonio Road, Palo Alto, CA 94303-4900, USA, August 1996. URL `http://www.sun.com/microelectronics/whitepapers/wpr-0013/index.html`. Demonstrates speedups of 2x to 5x on key networking kernels from use of the VIS instruction set.

Sun:1996:UVI

[Sun96b] Sun Microsystems. UltraSPARC: The Visual Instruction Set (VIS): On chip support for new-media processing. Technical Report WPR-0004, Sun Microsystems, 901 San Antonio Road, Palo Alto, CA 94303-4900, USA, 1996. URL `http://www.sun.com/microelectronics/whitepapers/wpr-0004; http://www.sun.com/microelectronics/whitepapers/wpr-0004/wpr-0004.pdf`.

Sun:2000:SAL

[Sun00] Sun Microsystems, 901 San Antonio Road, Palo Alto, CA 94303-4900, USA. *SPARC Assembly Language Reference Manual*, February 2000. URL `ftp://192.18.99.138/806-3774/806-3774.pdf`. Part Number 806-3774. See Appendix E.6 for UltraSPARC and VIS Instruction Set Extensions.

Sun:2002:VIS

[Sun02] Sun Microsystems. The VIS instruction set, version 1.0. White paper, Sun Microsystems, Network Circle Santa Clara, CA 95054, USA, June 2002. URL `http://www.sun.com/processors/vis/download/vis/vis_whitepaper.pdf; http://`

www.sun.com/processors/whitepapers/vis_wp_external.pdf.

Thakkar:1999:ISS

[TH99] Shreekant (Ticky) Thakkar and Tom Huff. The Internet Streaming SIMD Extensions. *Intel Technology Journal*, (Q2):8, May 17, 1999. URL http://developer.intel.com/technology/itj/q21999/articles/art_1.htm; http://developer.intel.com/technology/itj/q21999/pdf/simd_ext.pdf.

Thompson:1998:CPD

[Tho98] Tom Thompson. CPUs: PowerPC does blazing vector. *Byte Magazine*, 23(7):43–??, July 1998. CODEN BYTEDJ. ISSN 0360-5280 (print), 1082-7838 (electronic).

Tremblay:1996:UFI

[TO96] Marc Tremblay and J. Michael O'Connor. UltraSparc I: A four-issue processor supporting multimedia: Combining on-chip multimedia instructions with a high-performance, four-issue architecture. *IEEE Micro*, 16(2):42–50, March/April 1996. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). Presented at Hot Chips VII, Stanford University, Stanford, California, August 1995.

Tremblay:1996:VSN

[TONH96] Marc Tremblay, J. Michael O'Connor, Venkatesh Narayanan, and Liang He. VIS speeds new media processing — enhancing conventional RISC instruction sets to significantly accelerate media-processing algorithms. *IEEE Micro*, 16(4):10–20, July/August 1996. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Weiser:1996:TCP

[Wei96] Uri Weiser. Trade-off considerations and performance of Intel's MMX technology. In IEEE [IEE96], pages 147–156. ISBN ???? LCCN ????